



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al.

Docket No.: INF-135

Filed: 2/13/2004

Examiner: Andy Huynh

Serial No.: 10/777,128

Art Unit: 2818

Title: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant wishes to bring to the attention of the U.S. Patent and Trademark Office the information noted on the enclosed PTO Form PTO/SB/08A, which may be considered material to the examination of the above-identified application. A copy of the U.S. Patent cited is not being submitted.

This Information Disclosure Statement is submitted under 37 C.F.R. §1.97(d) together with a Statement under 37 C.F.R. §1.97(e), and a \$180.00 fee set forth in 37 C.F.R. §1.17(p) as this disclosure is being filed after notice of allowance, but before payment of the issue fee.

Please charge the required fee of \$180.00 and any additional amount, or credit any overpayment to Deposit Acct. No 50-1065 of the below mentioned firm.

12/21/2005 LWNDIH1 00000099 501065 10777128

01 FC:1806 180.00 DA

Respectfully submitted,

Ira S. Matsil
Attorney for Applicant
Reg. No. 35,272

Slater & Matsil, L.L.P.
17950 Preston Road, Suite 1000
Dallas, Texas 75252
Tel: (972) 732-1001
Fax: (972) 732-9218



Slater & Matsil, L.L.P.

Suite 1000
17950 Preston Road
Dallas, Texas 75252-5793
Phone: 972-732-1001 Facsimile: 972-732-9218

FACSIMILE COVER SHEET

To: Commissioner for Patents	Total Pages Sent: 5
Mail Stop Issue Fee	(including cover sheet)
Facsimile Number: 571-273-2885	Transmission Date: December 20, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al. Docket No.: INF-135
Serial No: 10/777,128 Art Unit: 2818
Date Filed: February 13, 2004
Title: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 571-273-2885 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Information Disclosure Statement (1 original and 1 copy)
- Statement Under 37 CFR 1.97(e) (1 page)
- Form PTO/SB/08A (1 page), with 1 reference cited

Respectfully submitted,

Anne Marie James
Legal Assistant

Confirmation Respectfully Requested

BEST AVAILABLE COPY

This facsimile is intended only for the use of the address named and contains legally privileged and/or confidential information. If you are not the intended recipient of this telecopy, you are hereby notified that any dissemination, distribution, copying or use of this communication is strictly prohibited. Applicable privileges are not waived by virtue of the document having been transmitted by Facsimile. Any misdirected facsimiles should be returned to the sender by mail at the address indicated on this cover sheet.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Schloesser, et al.

Serial No.: 10/777,128

Filing Date: 2/13/2004

Title: Architecture for Vertical Transistor
Cells and Transistor-Controlled Memory
Cells

Attorney Docket No.: INF-135

Examiner:

Andy Huynh

Group Art Unit:

2818

COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, VA 22313-1450

STATEMENT UNDER 37 CFR 1.97(e)

Sir:

The undersigned hereby certifies that either:

- (X) Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, not more than three months prior to the filing of the statement, or
- () No item of information contained in the Information Disclosure Statement
- was cited in a communication from a foreign patent office in a counterpart foreign application, and
- to the knowledge of the undersigned, after making reasonable inquiry, was known to an individual designated in 37 CFR 1.56 (c) more than three months prior to the filing of the Information Disclosure Statement.

Respectfully Submitted,

By

Ira S. Matsil

Attorney/Agent for Applicant

Reg. No.: 35,272

I hereby certify that this Correspondence is being deposited with the United States Postal service with sufficient postage for first class mail in an envelope address to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or the correspondence is being facsimile transmitted to the USPTO, on the date indicated below.

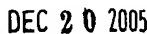
Date of Deposit: December 20, 2005

Typed Name: AnneMarie James

Signature:

Date: December 20, 2005

Telephone No.: 972-732-1001



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Sheet	1	of	
-------	---	----	--

[illegible][illegible]

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PAGE 5/5 * RCVD AT 12/20/2005 5:24:42 PM (Eastern Standard Time) * SVR:USPTO-EFXRF-6/32 * DNIS:2732885 * CSID:9727329218 * DURATION (mm-ss):01-34